Performance Benchmarking of Optical DAC Architectures under Realistic Electrical Driving

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***Abstract*—We present a comprehensive system-level comparison of optical digital-to-analog converter (oDAC) architectures—serial, multi-parallel, and 2S2P—against conventional MZM transmitters for data-center links, accounting for realistic electronic DAC impairments including bandwidth limitations and timing jitter.**

I. Introduction

Data-center networks (DCNs) must continue to increase capacity while reducing cost and energy per bit [1]. As symbol rates and modulation orders rise, single-wavelength transceivers face the well-known trade-off between bandwidth and effective number of bits (ENOB) in their electronic digital-to-analog and analog-to-digital converter (eDAC/eADC) interfaces [2]. Optical digital-to-analog converters (oDACs) address this bottleneck by generating multilevel optical signals directly in the photonic domain. Prior work spans serial (segmented) Mach–Zehnder modulator (MZM) schemes [3], [4] and parallelized designs [5], [6], including their experimental demonstrations [7], as well as two-serial two-parallel (2S2P) approaches [8] that combine the advantages of both designs. Yet rigorous system-level assessment of these oDAC architectures, especially in comparison with conventional transmitter architectures, remains limited.

In this paper, we compare three oDAC architectures with a conventional MZM-based transmitter for data-center coherent links. The comparison uses an experimentally validated electronic digital-to-analog converter (eDAC) model including finite resolution, timing jitter, bandwidth limitations, and electrical signal-to-noise ratio (SNR) degradation. The results show clear architecture-dependent performance differences.

II. Principle

The three oDAC architectures, namely the multi-parallel (MP), serial (segmented), and two-serial two-parallel (2S2P), for an optical pulse-amplitude modulation 8-level (oPAM8) implementation, are illustrated in Fig. 1 (a)-(c). For reference, we also include a conventional eDAC+MZM transmitter, shown in Fig. 1(d). Although all three oDACs generate high-order constellations from binary pulse-amplitude modulation (PAM2) drives, they operate differently. In each architecture, the MZM plays a different role, which changes the effective transfer function and leads to different link-performance outcomes.

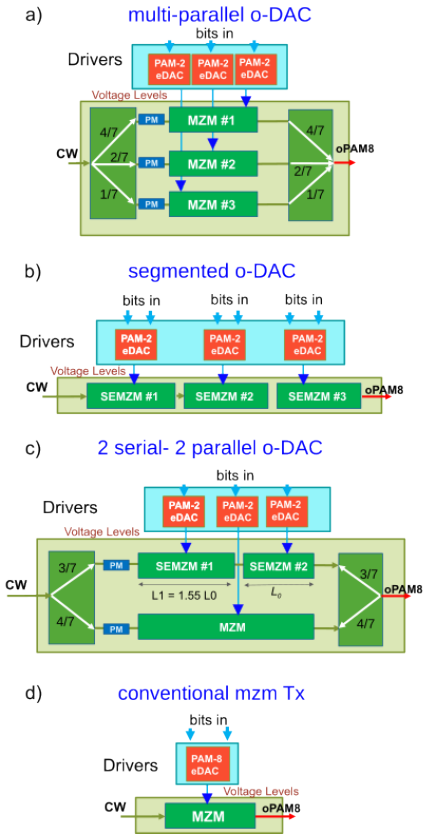

Fig. 1. oDAC-based building blocks for next-generation high-speed transmitters, illustrated for oPAM8; a) multi-parallel o-DAC, b) segmented o-DAC, c) 2 serial - 2 parallel o-DAC. Their performance is benchmarked against d) the conventional eDAC+MZM scheme

In the MP-oDAC scheme, shown in Fig. 1(a), several Mach–Zehnder modulators (MZMs) are arranged in parallel and operate as binary phase-shift keying (BPSK) phase gates. Each branch is driven by a binary signal and weighted through the splitter and combiner ratios. The output signal is obtained by coherently adding the weighted optical fields, with each branch contributing a ± 1 phasor. In this way, the multilevel optical PAM signal is generated linearly across the parallel branches. This approach offers two main advantages. First, it enables nearly equidistant constellation levels at full drive, without the modulation loss caused by drive back-off. Second, because each branch is binary-driven, the MZM transfer

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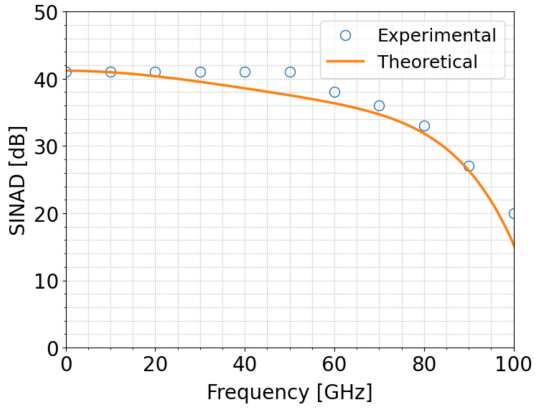

Fig. 2. Signal-to-noise-and-distortion ratio (SINAD) versus frequency of the electronic digital-to-analog converter (eDAC) model used in this work, fitted to published data for the Keysight MB8199B arbitrary waveform generator (AWG) DAC cores [11].

function can favorably reshape bandwidth-limited pulses and partially suppress driver noise. As a result, the optical levels are cleaner. Together, these effects give the MP-oDAC a 2R-like regenerative behavior and improve link performance.

In the serial architecture shown in Fig. 1(b), the MZM is divided into isolated push–pull segments driven by synchronized binary signals. The segments are weighted through their electrode lengths or drive amplitudes, so the total differential phase becomes a weighted sum of the binary inputs. This produces several discrete phase states, which the output coupler converts into multiple optical amplitude levels. Because the multilevel signal is formed inside the MZM in the phase domain, the waveform is shaped by the interferometer's sinusoidal phase-to-amplitude transfer function. As a result, the output levels are generally not equally spaced. More linear operation is possible only by reducing the drive voltage and keeping the MZM near its linear region, at the cost of significant modulation loss.

A hybrid architecture that combines the two previous operating principles is the two-serial two-parallel (2S2P) oDAC [8], shown in Fig. 1(c). It consists of two segmented MZM branches. Each branch first generates an oPAM2 or oPAM4 signal in a serial manner, and the two outputs are then coherently combined using programmable splitter and combiner ratios. Compared with the serial oDAC, the 2S2P architecture provides greater flexibility in setting the segment weights across the two branches, which allows the generation of nearly equidistant constellation levels, similar to those of MP-oDACs. At the same time, the sinusoidal transfer of the MZMs still provides pulse reshaping and partial noise suppression. In 2S2P, however, this benefit is level-dependent, so some constellation levels are improved more than others.

In the conventional transmitter, the multilevel electrical waveform is generated by a high-speed electronic digital-to-analog converter and then applied to a single MZM, see Fig. 1 d). This is the standard reference architecture considered in many coherent links. It requires a high-performance eDAC with sufficient bandwidth and ENOB. In this case, the full multilevel electrical waveform is directly exposed to electronic imperfections before optical modulation.

We evaluated all architectures under non-ideal electrical driving conditions. Specifically, we accounted for finite DAC resolution, timing jitter, bandwidth limitations, and electrical signal-to-noise ratio (SNR) degradation. To this end, we incorporated into our simulator the experimentally validated electronic digital-to-analog converter (eDAC) model of [9]. In this model, the frequency-dependent effective number of bits (ENOB) is obtained from the signal-to-noise-and-distortion ratio (SINAD) through the standard relation $\mathrm{ENOB} = (\mathrm{SINAD} - 1.76)/6.02$, where SINAD is in dB.

Figure 2 shows the adopted SINAD-versus-frequency characteristic. The model was fitted to published data for the Keysight MB8199B arbitrary waveform generator (AWG) DAC cores [11]. The fitting assumed a sampling rate of $256\,\mathrm{GSa/s}$ and an analog bandwidth of $80\,\mathrm{GHz}$. Although the DAC has a nominal 8-bit resolution, the fitted model yields an effective low-frequency ENOB of approximately 6.2 bits, a timing-jitter standard deviation of $\sigma_t = 40\,\mathrm{fs}$, and a magnitude response well described by a fourth-order Gaussian filter.

III. Simulation Setup and Results

Our system-level evaluation considered an unamplified data-center link with polarization multiplexing and coherent detection. The continuous-wave (CW) launch powers were 40 mW for the signal and 10 mW for the local oscillator (LO). Transmitter losses included the ideal splitter losses required by each oDAC configuration and a 1 dB waveguide loss per Mach–Zehnder modulator (MZM). To isolate the intrinsic behavior of the oDAC architectures, the channel was assumed linear, with no chromatic dispersion or fiber nonlinearities. The coherent receiver included shot noise, transimpedance-amplifier (TIA) thermal noise of 25 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$, a photodiode responsivity of 0.5 A/W, and an ideal optical hybrid. Performance is reported as link margin, defined as the negative of the maximum tolerable link loss in dB at a bit-error ratio (BER) of 2×10^{-2}, estimated over 640k transmitted symbols.

Figure 3 compares the link-margin performance of the different transmitter architectures for various modulation formats and symbol rates. In Fig. 3(a), the electrical signal-to-noise ratio (SNR) is fixed at 35 dB to isolate the impact of finite eDAC bandwidth and timing jitter. Each curve ends at the highest baud rate for which the bit-error ratio (BER) remains below 2×10^{-2}. Among the four architectures, the multi-parallel (MP) oDAC achieves the highest baud rates and the largest link margins. The two-serial two-parallel (2S2P) oDAC shows the second-best performance. The serial oDAC and the conventional eDAC+MZM transmitter perform less well, with the conventional architecture showing the fastest margin degradation at the highest baud rates and for 256-QAM.

Figure 3(b) shows the link margin as a function of electrical signal-to-noise ratio (SNR) at 100 GBaud. In all cases, the link margin increases monotonically with SNR. However, the multi-parallel (MP) oDAC consistently provides the highest margin across the full SNR range, reaching a given target margin at a lower electrical SNR than the other architectures.

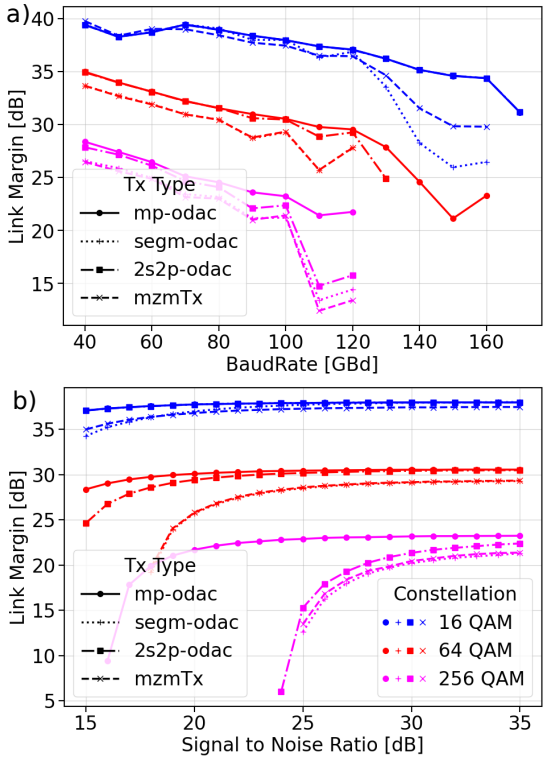

Fig. 3. Performance comparison of the four transmitter architectures. (a) Link margin versus baud rate at electrical SNR = 35 dB. (b) Link margin versus electrical SNR at 100 GBaud. (c) Single-quadrature eye diagrams for 256-QAM at 100 GBaud and electrical SNR = 35 dB.

The 2S2P-oDAC again follows closely, while the serial oDAC and the conventional eDAC+MZM transmitter require higher SNR to achieve the same performance. This ranking remains the same at both low and high SNR values.

The superior performance of MP-oDAC arises from its binary pulse-amplitude modulation (PAM2) branch driving and coherent weighted field addition. Each branch switches between two opposite phase states, which makes the architecture less sensitive to eDAC bandwidth and effective number of bits (ENOB) limitations. In addition, the Mach–Zehnder modulators (MZMs) reshape the binary pulses in a favorable way, rather than distorting a multilevel waveform as in the serial oDAC and the conventional eDAC+MZM transmitter. This behavior also leads to partial suppression of electrical noise through a 2R-like effect. The eye diagrams in Fig. 4 confirm this trend: the MP-oDAC case shows a larger vertical opening and cleaner crossings, indicating reduced intersymbol interference (ISI) and improved per-level SNR.

IV. Conclusions

We presented a system-level comparison of three optical digital-to-analog converter (oDAC) architectures,and benchmarked them against a conventional electronic digital-to-analog converter plus Mach–Zehnder modulator (eDAC+MZM) transmitter for data-center coherent links. By including realistic eDAC impairments, such as timing jitter, bandwidth limitations, and finite effective number of bits (ENOB), we showed that the way each architecture

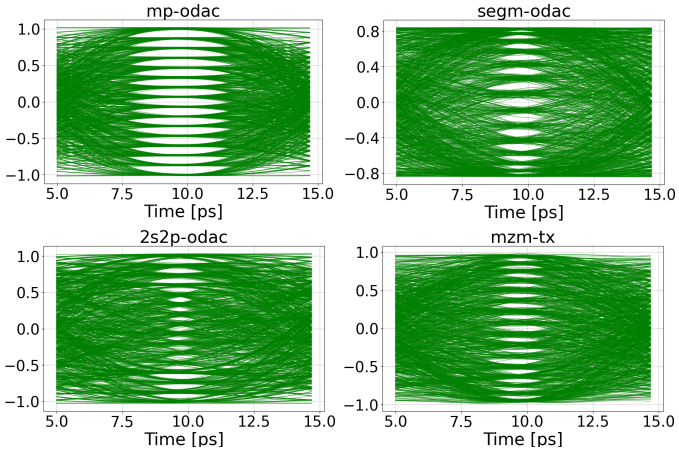

Fig. 4. 256-QAM single-quadrature eyes at 100 GBaud, SNR = 35 dB; MP-oDAC shows wider openings.

uses the MZM transfer function leads to clear performance differences. MP-oDAC achieves the highest link margins because of its 2R-like regenerative behavior, which mitigates electrical impairments. The 2S2P architecture offers a good compromise between performance and implementation flexibility. These results provide practical guidance for selecting an oDAC architecture based on link requirements and available driver technology.

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